Hot-Carrier and Soft-Breakdown Effects on VCO Performance

Enjun Xiao, *Student Member, IEEE*, J. S. Yuan, *Senior Member, IEEE*, and Hong Yang

***Abstract*—This paper systematically investigates the hot-carrier- and soft-breakdown-induced performance degradation in a CMOS voltage-controlled oscillator (VCO) used in phase-locked-loop frequency synthesizers. After deriving the closed-form equations to predict phase noise and VCO gain, we relate VCO RF performance such as phase noise, tuning range, and gain of VCO subject to electrical stress. The circuit degradations predicted by analytical model equations are verified by SpectraRF simulation using parameters extracted from the experimental data of 0.16-μm CMOS technology. BERT simulation results give VCO performance degradations versus operation time.**

***Index Terms*—Circuit reliability, dielectric breakdown, hot carriers, MOSFETs, phase-locked loops, phase noise, timing jitter, voltage-controlled oscillators (VCOs).**

I. Introduction

As CMOS device sizes shrink, the channel electric field increases and the hot-carrier (HC) effect becomes more significant [1]. When the oxide is scaled down to less than 3 nm, soft breakdown (SBD) often takes place [2]–[4]. As a result, oxide trapping and interface generation cause long-term performance drift and related reliability problems in devices and circuits.

A voltage-controlled oscillator (VCO) is the most important circuit in the phase-locked loop (PLL). It dominates almost all spectral purity performance of a frequency synthesizer. It is desirable for the VCO to generate low-noise signal with sufficient output power, wide tuning range, and high stability. However, the VCO performance is very sensitive to the variation of device parameters. The experimental results show that device performance is degraded significantly subject to HC stress and SBD [5]. Therefore, it is anticipated that the VCO circuit performance is degraded by hot electron stress and oxide SBD.

In this paper, the device performance drifts due to HC and SBD are examined experimentally by measuring threshold voltage, mobility, and transconductance before and after stress for 0.16-μm CMOS technology. Phase noise, tuning range, and gain degradations of a CMOS five-stage ring-oscillator VCO are systematically evaluated.

II. Device Degradation Due to HC and SBD Stress

To examine the HC and SBD effects, gate and substrate currents are measured, respectively, with the device overstress to reduce the characterization time. The impact of HC and SBD can be characterized as the degradation of major device parameters such as threshold voltage and mobility. The combination effect of HC and SBD is indicted by experimental results.

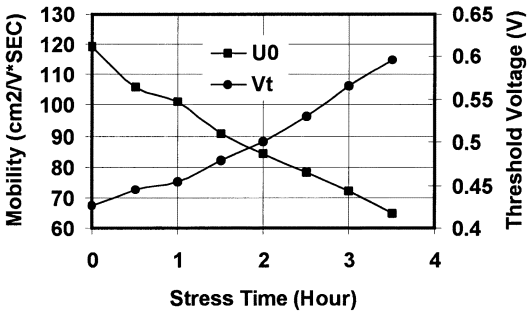

Fig. 1. Threshold voltage and mobility degradation versus stress time.

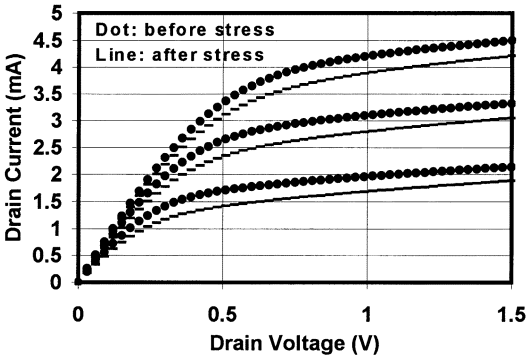

Fig. 2. Drain current degradation versus stress time.

The devices tested are 0.16-μm technology nMOSFETs. The oxide thickness is 2.4 nm and the gatewidth is 50 μm. Many transistors are tested to verify the statistical variance. The wafer is tested with a Cascade 12000 Probe Station and Agilent 4156B Precision Semiconductor Parameter Analyzer. The gate and drain voltages used for overstress are at 2.6 V and then measured at gate and drain voltages of 0.85 and 1.5 V, respectively, for reasonable operating condition. The source and bulk are grounded. For N-channel devices; the measured threshold voltage increases with stress time because of electron trapping and the measured mobility decreases due to the increase of interface state generation. This is verified by the degradation of the extracted parameters of the BSIM3v3 model. As seen in Fig. 1, the threshold voltage increases by 40% and the mobility decreases by 45% after 4 h of overstress. The drain current decreases after stress due to the degradation of threshold voltage and mobility. The drain current degradation is shown in Fig. 2.

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The authors are with the Chip Design and Reliability Laboratory, School of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL 32816 USA (e-mail: enjunx@yahoo.com).

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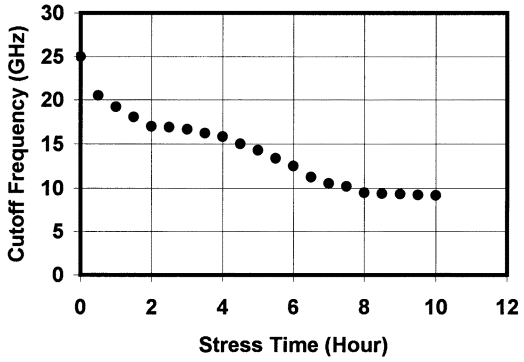


Fig. 3. Cutoff frequency degradation subject to stress.

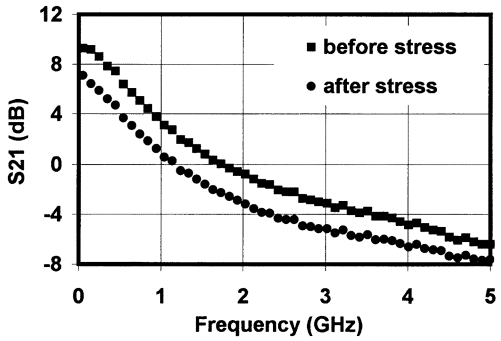


Fig. 4. S_{21} as a function of stress time.

The SBD and HC effects also degrade the RF parameters of CMOS devices. The same wafer is stressed and probed with a Cascade 12000 Probe Station and the RF parameters are examined using an Agilent 8510C Network Analyzer. The device S-parameters are measured and cutoff frequency of oscillation is extracted before and after stress. From the experimental data, S_{11} and S_{21} degrade significantly after stress and the cutoff frequency decreases greatly as well. The measured cutoff frequency and S_{21} degradations are displayed in Figs. 3 and 4, respectively.

III. Analytical Derivation

Phase noise and jitter in VCOs have been studied [6]–[11]. The VCO RF performance degradations are predicted by evaluating the dc parameter degradations of the transistors. The major parameters for VCOs are phase noise, tuning range, and gain. In order to predict the degradation of the VCO after stress, a five-stage ring VCO composed of five fully differential delay stages is examined. As shown in Fig. 5, each delay cell consists of NMOS differential pairs ($M2$ and $M3$) with PMOS resistive loads ($M0$ and $M1$). The biasing current is provided by $M4$ and $M5$. The gate voltage V_G is controlled carefully by a replica biasing circuit (not shown here) so that the PMOS transistors are working in the linear region and the voltage swing is kept constant. The purpose of derivation is to express VCO phase noise and jitter as functions of device parameters [12], [14]. The major concerns here are the device channel thermal noise sources and their impact on the VCO timing jitter. Flicker noise is not considered here because it will be filtered out by the PLL bandwidth at low frequency.

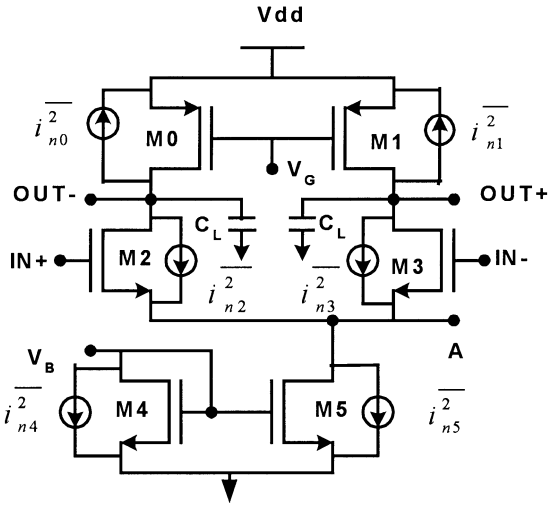


Fig. 5. Delay cell with channel thermal noise sources.

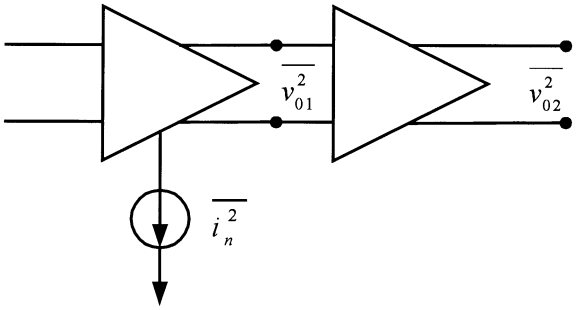


Fig. 6. Noise model.

The NMOS and PMOS transistors are working in the saturation and linear regions, respectively, whose channel thermal noise current power spectral densities are given by

$$\overline{i_{n\mathrm{NMOS}}^2} = 4kT\gamma_n g_m \Delta f \quad (1)$$

$$\overline{i_{n\mathrm{PMOS}}^2} = 4kT\gamma_p g_d \Delta f \quad (2)$$

where g_m is the transconductance, γ_n is the noise factor of the NMOS transistors, g_d is the drain-to-source transconductance, and γ_p is the noise factor of the PMOS transistors.

To analyze the effect of device channel thermal noise on the output noise, the equivalent-circuit model, shown in Fig. 6, is used. The contributions of every device noise source are different for different working phases of the delay stage. For differential pair $M2$ and $M3$ during switching, each side switches from fully off to on and g_m changes dramatically; thus, their noise contribution is not a constant. $M4$ and $M5$ contribute to the output noise when the differential pair is working in the balanced state. $M0$ and $M1$ noise always contributes to the output. The noise contributions are approximately divided into two constant regions. In the first region, the differential pairs are switching and the noise sources for the NMOS differential pair and PMOS resistive loads make noise contributions. In the second region, the differential pairs have completed switching and the noise contributions include the noise sources for PMOS resistive loads and the current source.

The equivalent circuit for each delay stage is shown in Fig. 7 and R_L is the equivalent output resistance. To find the output

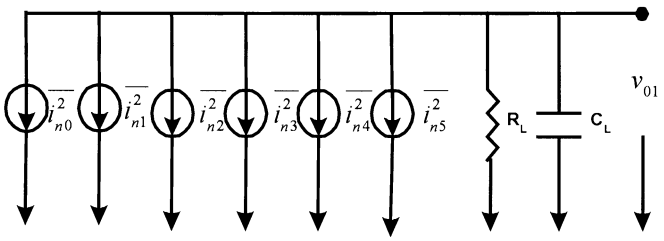


Fig. 7. Equivalent circuit for noise analysis.

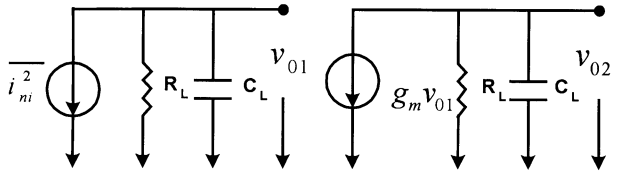


Fig. 8. Circuit model considering the inter-stage effect.

voltage noise $\overline{v_{01}^2}$, the autocorrelation functions for each device noise could be obtained. Suppose that the device noises are uncorrelated, the total output noise is then obtained by adding each device noise contribution.

First, the inter-stage amplification is ignored. From Fig. 7, the autocorrelation function of the output voltage noise is calculated using (3) as follows:

$$R_v(t_1,t_2) = R_i(t_1,t_2) \otimes h(t_1) \otimes h(t_2) \tag{3}$$

where $h(t) = 1/C_L \cdot e^{-t/\tau_D}$, $R_i(t_1,t_2) = 2kT\gamma g_m \delta(\tau)$ during switching and $\tau_D = R_L C_L$ is time constant for the output capacitance load.

The voltage noise variance equals to the autocorrelation function of the output voltage noise when $t_1 = t_2$ or $\tau = t_1 - t_2 = 0$. The contribution of each device noise source is obtained by calculating (3) for each device.

For $M2$ and $M3$, $\overline{v_0^2} = (kT\gamma_n G/C_L)(1 - e^{-2t/\tau_D})$ and G is the gain of delay stage.

For $M0$ and $M1$, $\overline{v_0^2} = kT\gamma_p/C_L$.

For $M5$ and $M6$, $\overline{v_0^2} = (kT\gamma_n G/C_L)\sqrt{2X_1}(1 + X_2)e^{-2t/\tau_D}$, where X_1 is the size ratio of $M5$ and $M3$, and X_2 is the size ratio of $M4$ and $M5$.

The output voltage noise could be obtained by adding each device noise contribution. The inter-stage impact is also considered. The equivalent circuit is shown in Fig. 8.

Using the similar method above, the output voltage noise due to the inter-stage impact is obtained as follows:

$$\overline{v_0^2} = \frac{kT\gamma_n G^3}{2C_L}\left[1 - \left(1 + \frac{4t_D}{\tau_D} + \frac{8t_D^2}{\tau_D^2}\right)e^{-2t/\tau_D}\right]. \tag{4}$$

By analyzing the impact of every device channel thermal noise on the output noise, including the time-varying effect and inter-stage amplification, the output noise of single delay cell is expressed as

$$V_n^2 = \frac{kT}{2}\frac{G^2\alpha^2}{C_L} \tag{5}$$

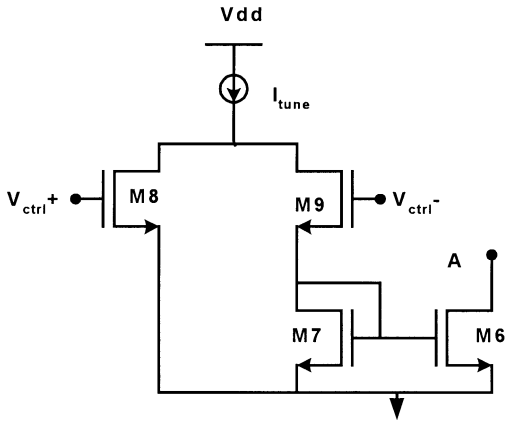


Fig. 9. Control circuit.

where G is the gain of the delay cell, and α is the noise factor given by

$$\alpha^2 = 2\gamma_p + 2\gamma_n G\left\{1 + \left[\sqrt{\frac{X_1}{2}}(1 + X_2) - 1\right] \cdot \left(1 + \frac{4t_D}{\tau_D} + \frac{8t_D^2}{\tau_D^2}\right)e^{-4t_D/\tau_D}\right\}. \tag{6}$$

The timing jitter for single delay stage is given by

$$\sigma_D^2 = \frac{kT}{2}\frac{G^2}{I_{ss}^2}\alpha^2 C_L. \tag{7}$$

For an n-stage ring oscillator, the output frequency is $f_0 = 1/(2nt_D)$ and the output timing jitter is $\sigma_{f_0}^2 = 2n\sigma_D^2$ given by

$$\sigma_{f_0}^2 = \frac{kT}{2}\frac{G}{I_{SS}(V_{gs} - V_{Tn})}\frac{\alpha^2}{f_0}. \tag{8}$$

The output phase noise of a ring oscillator is thus

$$\begin{aligned} L\{f_m\} &= \frac{f_0}{f_m^2}\frac{\sigma_{f_0}^2}{T_0^2} \\ &= \left(\frac{f_0}{f_m}\right)^2 \frac{kTG\alpha^2}{\mu C_{OX}\left(\frac{W}{L}\right)_{M5}(V_{gs3} - V_{Tn})(V_{gs5} - V_{Tn})^2}. \end{aligned} \tag{9}$$

For a PLL, the oscillator frequency is controlled by the bias current corresponding to the bias voltage V_B. The VCO gain corresponds to a small change of output frequency caused by the control voltage with respect to the phase difference between the reference frequency and the $1/N$ of the VCO frequency. The differential control circuit is shown in Fig. 9. The input is from the differential output of charge pump and loop filter.

The VCO gain is given by [14]

$$G_{\mathrm{VCO}} = \frac{\partial f_0}{\partial V_{\mathrm{ctrl}}} \cong \frac{\partial f_0}{\partial I_t} g_m X_t \tag{10}$$

where I_t is the tuning current and X_t is the size ratio of $M6$ and $M7$.

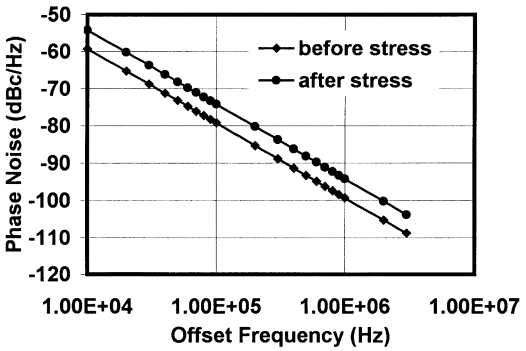


Fig. 10. Predicted phase noise versus offset frequency.

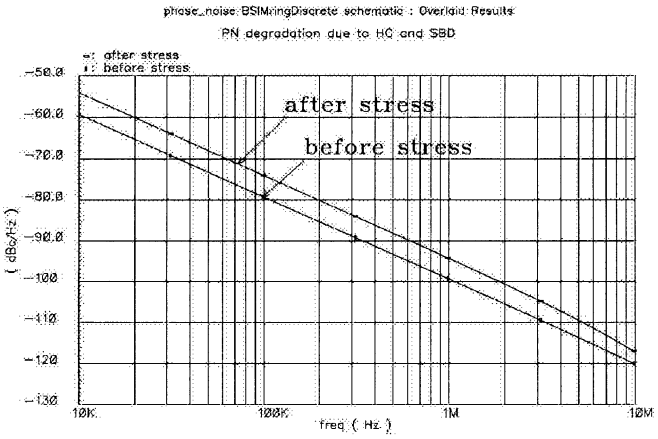


Fig. 11. Simulated phase noise versus offset frequency.

IV. VCO Degradations Subject to Stress

Using the analytical equations derived in Section III, the VCO performance degradation due to HC and SBD effects are examined. A five-stage ring oscillator is considered. First, the wafer of the 0.16-μm CMOS process is stressed on a Cascade 12000 Probe Station and then measured via an Agilent 8510C Network Analyzer. The measured parameters are used in both the model file for Cadence SpectraRF simulation and our analytical model. The predicted phase noise change due to HC and SBD effects is shown in Fig. 10 and the simulation results are shown in Fig. 11. It is clear that the phase noise increases by approximately 6 dB after stress. Good agreement between the model predictions and simulation results are obtained.

The VCO tuning range changes dramatically after stress. From Fig. 12, the VCO center frequency drifts approximately 55 MHz and the tuning range decreases approximately 20%, from 344 to 274 MHz after about 2.25 h of stress.

From Fig. 13, the VCO gain is reduced by 24% after 2.25 h of stress. The above figures show that the HC- and SBD-induced effects degrade the VCO performance dramatically. After stress, the phase noise will increase and the center frequency, tuning range, and gain will decrease. It is expected that the VCO performance degradation would affect the performance of the PLL, and then the whole receiver performance. The increased phase noise would degrade the selectivity of the receiver and the lowered tuning range and gain will impact the locking time and stability of the receiver.

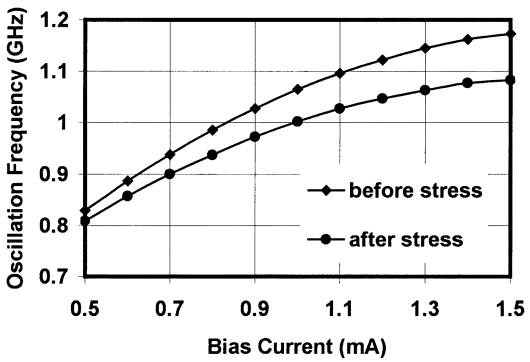


Fig. 12. Oscillation frequency versus bias current.

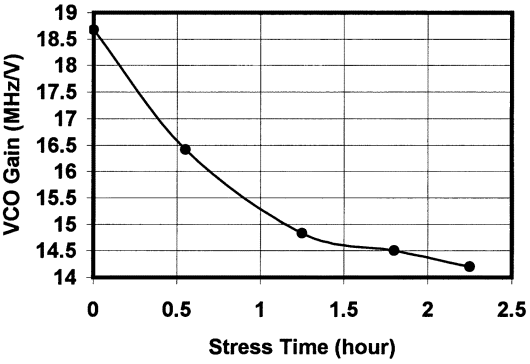


Fig. 13. VCO gain as a function of stress time.

The normalized VCO phase noise and gain degradations subject to stress can be written as a function of shifting of threshold voltage and mobility as follows:

$$\frac{\Delta L\{f_m\}}{L\{f_m\}} = \frac{1}{\left(1+\frac{\Delta\mu}{\mu}\right)\left(1-\frac{\Delta V_{Tn}}{V_{gs3}-V_{Tn}}\right)\left(1-\frac{\Delta V_{Tn}}{V_{gs5}-V_{Tn}}\right)^2} - 1 \tag{11}$$

$$\frac{\Delta G_{\rm VCO}}{G_{\rm VCO}} = \left(1+\frac{\Delta\mu}{\mu}\right)\left(1-\frac{\Delta V_{Tn}}{V_{gs}-V_{Tn}}\right) - 1. \tag{12}$$

It is clear from (11) and (12) that $V_{gs}-V_{Tn}$ for each delay cell should be chosen as large as possible to reduce the degradation effect, but needs to be small enough to guarantee the gain greater than one to sustain oscillation.

V. VCO Aging Prediction

The VCO degradations due to HC and SBD effects before and after stress are demonstrated based on overstress measurement. To examine the VCO performance under normal operating or stress condition, the BERT aging simulation is performed. BERT is a circuit reliability simulator that consists of pre- and post-processors linked with a SPICE simulator. It is developed to predict CMOS circuit lifetime accurately for the circuits suffering HC and breakdown [13].[1] It is consistent with the

[1]The software is now called RelXpert by Celestry, San Jose, CA.

normal SPICE modeling technique and has very high accuracy on the condition that all the parameters provided are accurate.

To calculate the HC-induced device degradation, BERT defines a parameter Age that quantifies the amount of HC stress. Take NMOS as an example. Under dc conditions, Age is calculated as At, where t is time and

$$A = \frac{I_{\rm ds}}{HW}\left(\frac{I_{\rm sub}}{I_{\rm ds}}\right)^m \tag{13}$$

where H is a constant, m is an acceleration factor, W is the device channel width, and $I_{\rm sub}$ and $I_{\rm ds}$ are the substrate and drain currents, respectively.

To obtain the Age under ac conditions, one can use the quasi-static approximation as

$$Age = N\int_0^T \frac{I_{\rm ds}}{HW}\left(\frac{I_{\rm sub}}{I_{\rm ds}}\right)^m dt \tag{14}$$

where T is a specified period and N is the number of periods.

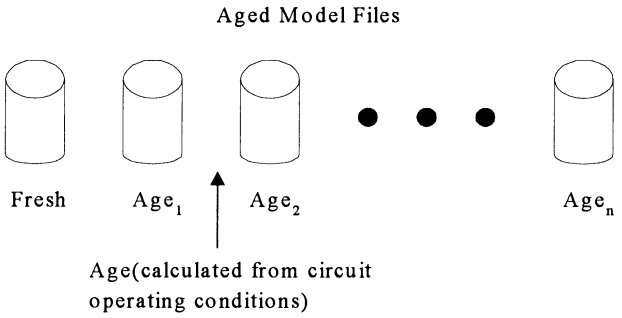
HC-induced device degradation in MOSFETs is usually measured by the change in transconductance $\Delta g_m/g_m$, drain current $\Delta I_d/I_d$, threshold voltage shift ΔV_T, etc. The degradation, generalized by using the symbol ΔD, is given by

$$\Delta D = Age^n. \tag{15}$$

ΔD can be further generalized to the degradation in any of the transistor's SPICE model parameters. The degradation ΔD as a function of Age can be extended to the "aging" of transistor model parameters. Thus, degraded SPICE models can be constructed for circuit aging simulation to examine circuit behavior after HC degradation in MOS transistors.

SPICE model parameters are extracted from a device at a number of dc stress intervals. These models form a set of "aged" model files. Each of the files represents the transistor behavior after HC stress. The amount of stress is given by the Age parameter. During the ac aging simulation, the Age for each individual device is calculated. Using Age as a basis, a degraded transistor model for each device from the "aged" model files can be constructed by either interpolation or regression from these files in the linear–linear, linear–log, or log–log relations. The "aged" model file method of calculating "aged" SPICE model parameter is graphically shown in Fig. 14. The values p_1, p_2, and p_3 are the degraded model parameters in SPICE model files with Age_1, Age_2, and Age_3, respectively. P_i and P_r are the respective model parameters if interpolation or regression is selected.

SPICE model parameters are extracted from 0.16-μm CMOS devices at a number of dc stress intervals. These models form a set of aged dc model files. By means of quasi-static approximation, aged ac models for every transistor in the VCO circuit can be constructed and used for circuit aging simulation. Shown in Figs. 15 and 16 are the simulated VCO phase noise and tuning range degradations. It is shown that the VCO performance is degraded significantly in the first two years and then the degradation slows down. For a ten-year period, the phase noise degradation is approximately 3 dB. The VCO tuning range is decreased from 250 to 180 MHz.



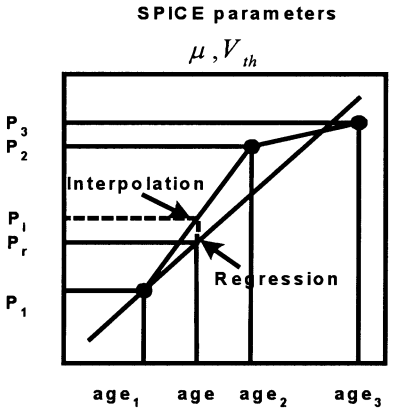


Fig. 14. Aged model interpretation.

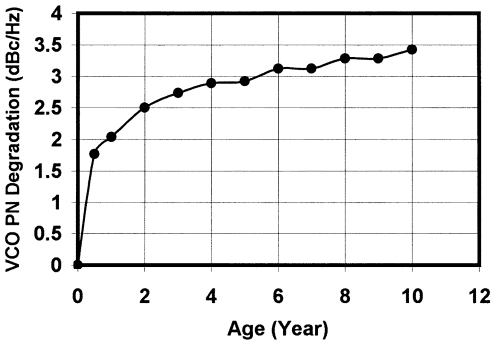


Fig. 15. VCO phase noise versus operation time.

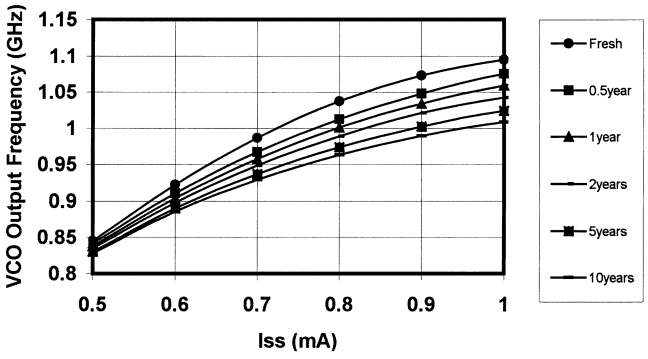


Fig. 16. VCO tuning range versus operation time.

VI. Summary

The analytical equations to predict the VCO performance degradation subject to hot electron stress and oxide SBD have been derived. Device parameters of 0.16-μm CMOS technology have been measured before and after stress. The analytical model predictions of VCO performance have been compared with SpectreRF simulation. Good agreement between the model predictions and simulation results has been obtained. The phase noise has increased and VCO gain and tuning range have decreased with respect to stress time. BERT aging simulation of VCO phase noise and tuning range degradations under the normal circuit operation condition for ten years of stress have been demonstrated. These results are useful for RF circuit designers to build more reliable RF circuits.

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Enjun Xiao (S'01) received the B.S. degree in electrical engineering from Shandong University, Jinan, China, in 1983, M.S. degree in communication and electronic systems from The Second Academy of China Aero-Space Corporation (CASC), Beijing, China, in 1988, and is currently working toward the Ph.D. degree in electrical engineering at the University of Central Florida (UCF), Orlando.

From 1988 to 1999, he was a Senior Engineer with CASC, where he was responsible for mixed-signal circuits and systems design. Since 1999, he has been a Research Assistant with the Chip Design and Reliability Laboratory, UCF, where he is involved in the CMOS RF integrated circuit (IC) design for wireless communications and CMOS device and circuit reliability.

J. S. Yuan (S'85–M'88–SM'92) received the M.S. and Ph.D. degrees from the University of Florida, Gainesville, in 1984 and 1988, respectively.

In 1990, he joined the faculty of the University of Central Florida (UCF), Orlando, after one year of industrial experience with Texas Instruments Incorporated, where he was involved with 16-MB CMOS DRAM design. He is currently a Professor and Director of the Chip Design and Reliability Laboratory, School of Electrical Engineering and Computer Science, UCF. He has authored or coauthored over 150 papers in referred journals and conference proceedings in the area of semiconductor devices and circuits. He authored *Semiconductor Device Physics and Simulation* (New York: Plenum, 1998) and *SiGe, GaAs and InP Heterojunction Bipolar Transistors* (New York: Wiley, 1999). Since 1990 he has conducted many research projects funded by the National Science Foundation (NSF), Motorola, Harris, Lucent Technologies, National Semiconductor, and Theses Logic. He is a reviewer for *Solid-State Electronics*. He is an Associate Editor of the *International Journal of Modeling and Simulation* He is listed in *Who's Who in American Education* and *Who's Who in Science and Engineering*.

Dr. Yuan is a member of Eta Kappa Nu and Tau Beta Pi. He is the chairman of the Electron Device Chapter, IEEE Orlando Section. He is an editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY. He is a reviewer for the IEEE TRANSACTIONS ON ELECTRON DEVICES and IEEE ELECTRON DEVICE LETTERS. He has been the recipient of numerous awards, including the 2002 UCF Distinguished Researcher Award, the 1995 Outstanding Engineering Award, the 1995 IEEE Orlando Section MMII, the 1995 UCF TIP Award, UCF, and the 1993 Outstanding Engineering Educator Award, IEEE Orlando Section and Florida Council.

Hong Yang was born in Xiangtan, China, in 1972. He received the B.S. degree in applied physics from the Central South University of Technology, Changsha, China, in 1994, the M.S.E.E. degree from University of Central Florida (UCF), Orlando, in 2002, and is currently working toward the Ph.D. degree at the UCF.

Since 2000, he has been a Research Assistant with the Chip Design and Reliability Laboratory, UCF. His research is focused on CMOS reliability issues including HC and dielectric breakdown and their impact on digital and RF circuits.